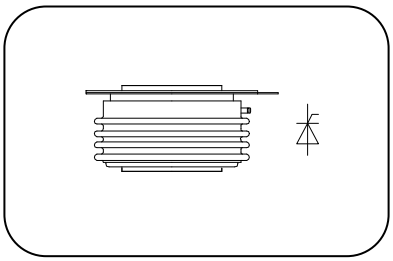
DYNSEM

DST550 /14E
PHASE CONTROL THYRISTOR

Features
- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

Typical Applications
- AC controllers
- DC and AC motor control
- Controlled rectifiers

$I_{T(AV)}$	555A	
V_{DRM}/V_{RRM}	1100~1800V	
I_{TSM}	8.0	kA
I^2t	320	10^3A^2S



SYMBOL	CHARACTERISTIC	TEST CONDITIONS		T_j(°C)	VALUE			UNIT
					Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled,	T_C= 55°C	125			800	A
			T_C=85°C				555	
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM}&V_{RRM} tp=10ms V_{DSM}&V_{RSM}= V_{DRM}&V_{RRM}+100V		125	1100		1800	V
I_{DRM} I_{RRM}	Repetitive peak current	V_R= V_{DRM} V_R= V_{RRM}		125			30	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}		125			8.0	kA
I^2t	I^2T for fusing coordination						320	A^2s*10^3
V_{TO}	Threshold voltage			125			0.82	V
r_T	On-state slop resistance						0.57	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=1500A, F=7.0kN		25			1.65	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67V_{DRM}		125			1000	V/μs
di/dt	Critical rate of rise of on-state current	V_{DM}= 67%V_{DRM} to 800A, Gate pulse t_r ≤0.5μs I_{GM}=1.5A Repetitive		125			100	A/μs
Q_{rr}	Recovery charge	I_{TM}=800A,tp=2000μs, di/dt=-20A/μs, V_R =50V		125		1030		μC
I_{GT}	Gate trigger current	V_A=12V, I_A=1A		25	35		250	mA
V_{GT}	Gate trigger voltage				0.8		2.5	V
I_H	Holding current				20		200	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=0.67V_{DRM}		125	0.3			V
$R_{th(j-c)}$	Thermal resistance Junction to case	At 180° sine, double side cooled Clamping force 7.0kN					0.045	°C /W
$R_{th(c-h)}$	Thermal resistance case to heat sink						0.010	
m	Mounting force				5.3		10	kN
T_{stg}	Stored temperature				-40		140	°C
W_t	Weight					80		g
Outline	KT25aT							

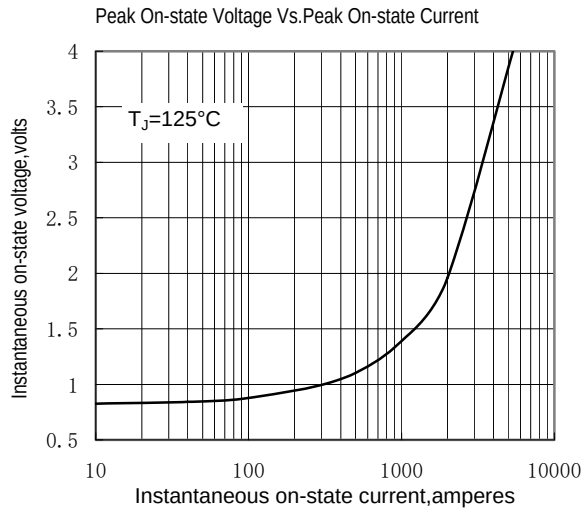


Fig.1

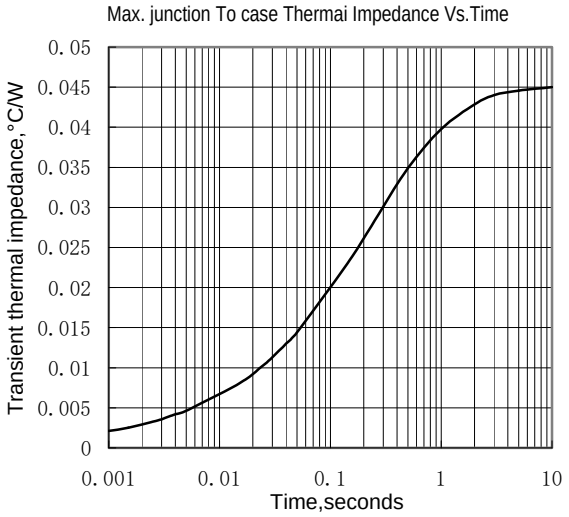


Fig.2

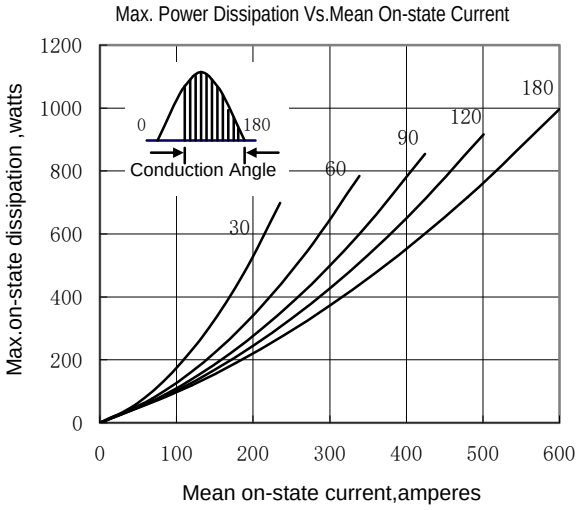


Fig.3

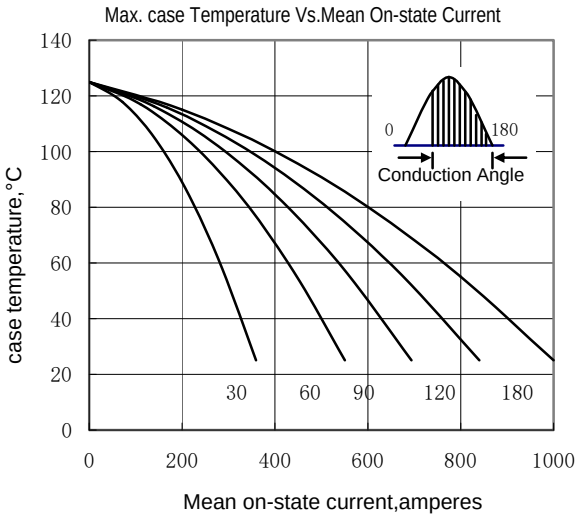


Fig.4

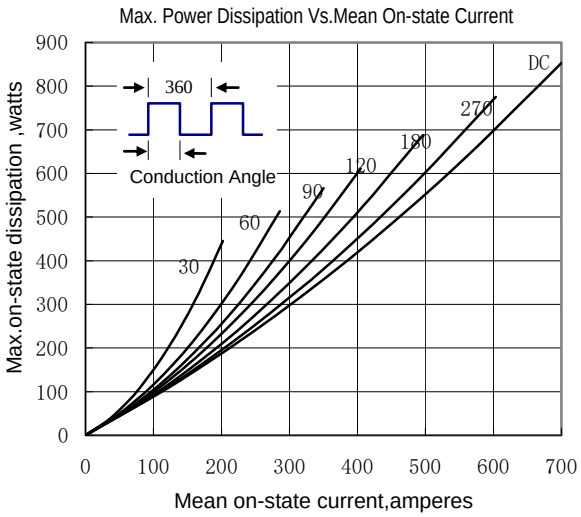


Fig.5

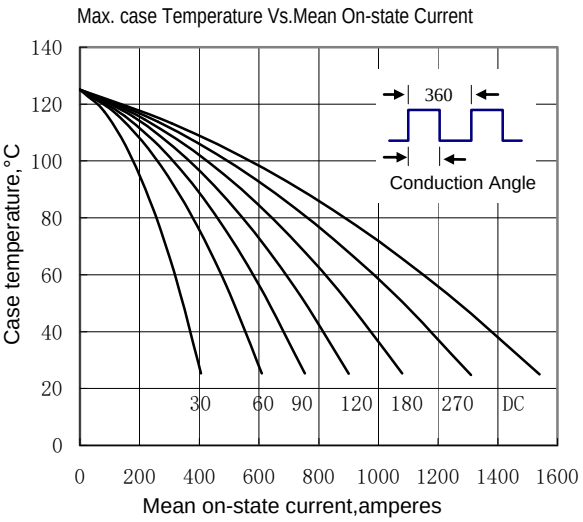


Fig.6

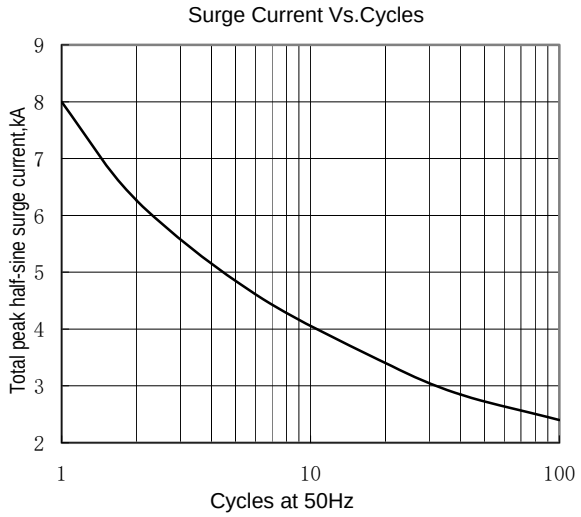


Fig.7

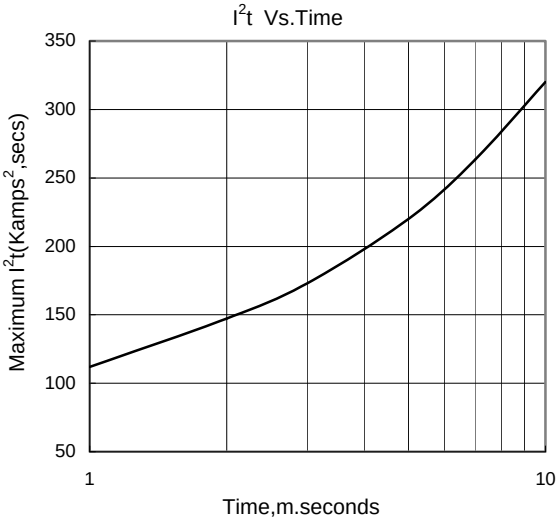


Fig.8

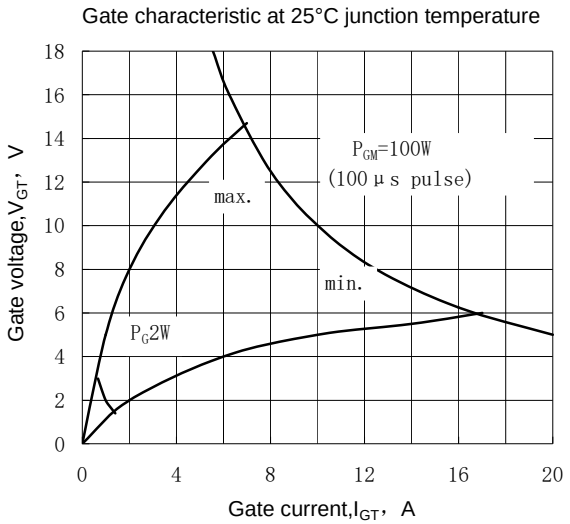


Fig.9

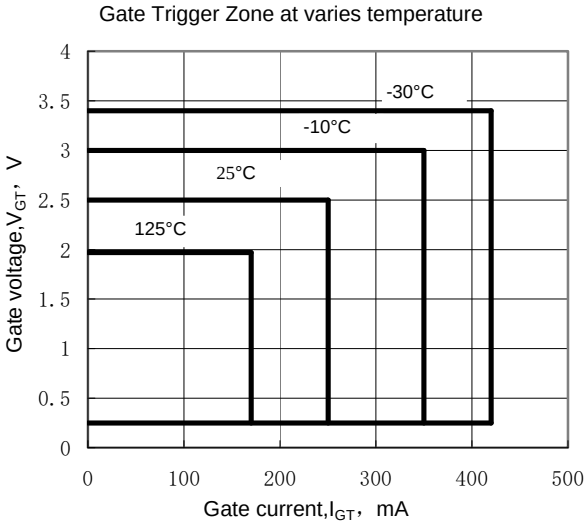


Fig.10

Outline: