



DSPACK 2

Features:

- Isolated mounting base 4000V~
- Pressure contact technology with Increased power cycling capability
- Space and weight saving
- UL Recognized

Typical Applications

- AC/DC Motor drives
- Various rectifiers
- DC supply for PWM inverter

V_{DSM}, V_{RSM}	V_{DRM}, V_{RRM}	Type & Outline
2700V	2600V	DSKT 135/26
2900V	2800V	DSKT 135/28
3100V	3000V	DSKT 135/30
3300V	3200V	DSKT 135/32
3500V	3400V	DSKT 135/34
3700V	3600V	DSKT 135/36

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	$T_J(^{\circ}C)$	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled, $T_c=85^{\circ}C$	125			135	A
$I_{T(RMS)}$	RMS on-state current		125			212	A
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			25	mA
I_{TSM}	Surge on-state current	10ms half sine wave	125			3.60	KA
I^2t	I^2t for fusing coordination	$V_R=60\%V_{RRM}$				65	$A^2s \cdot 10^3$
V_{TO}	Threshold voltage		125			0.94	V
r_T	On-state slope resistance					2.40	mΩ
V_{TM}	Peak on-state voltage	$I_{TM}=410A$	25			2.35	V
dv/dt	Critical rate of rise of off-state voltage	$V_{DM}=67\%V_{DRM}$	125			800	V/μs
di/dt	Critical rate of rise of on-state current	$I_{TM}=270A$, Gate source 1.5A $t_r \leq 0.5\mu s$ Repetitive	125			100	A/μs
I_{GT}	Gate trigger current	$V_A=12V, I_A=1A$	25	30		150	mA
V_{GT}	Gate trigger voltage			0.8		2.5	V
I_H	Holding current			20		150	mA
V_{GD}	Non-trigger gate voltage	$V_{DM}=67\%V_{DRM}$	125	0.2			V
$R_{th(j-c)}$	Thermal resistance Junction to case	Single side cooled per chip				0.170	$^{\circ}C/W$
$R_{th(c-h)}$	Thermal resistance case to heat sink	Single side cooled per chip				0.08	$^{\circ}C/W$
V_{iso}	Isolation voltage	50Hz, R.M.S, $t=1min, I_{iso}: 1mA(MAX)$		4000			V
F_m	Thermal connection torque (M6)				6.0		N·m
	Mounting torque (M6)				6.0		N·m
T_{stg}	Stored temperature			-40		125	$^{\circ}C$
W_t	Weight				305		g
Outline	DSPACK 2						

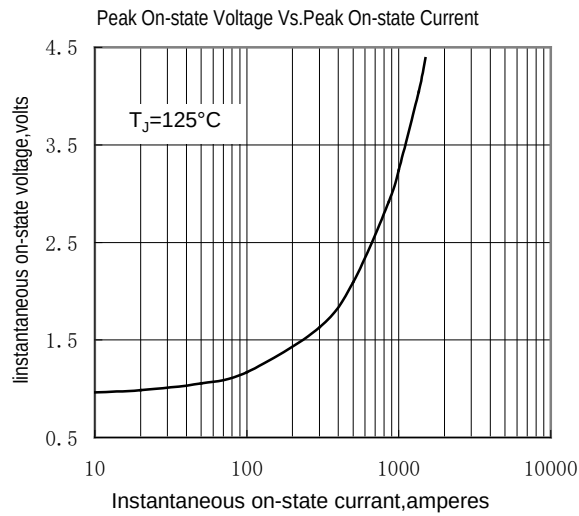


Fig.1

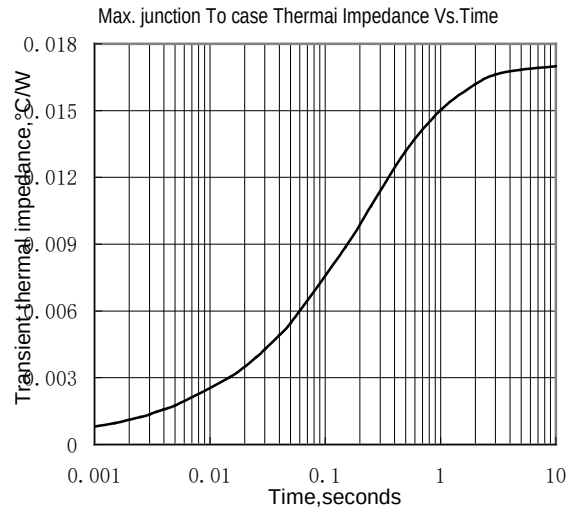


Fig.2

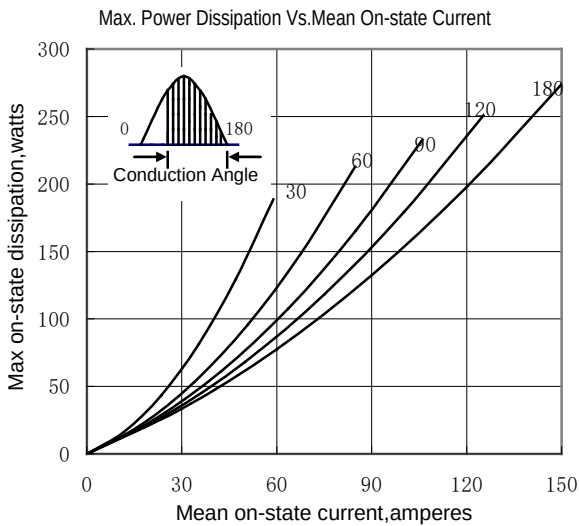


Fig.3

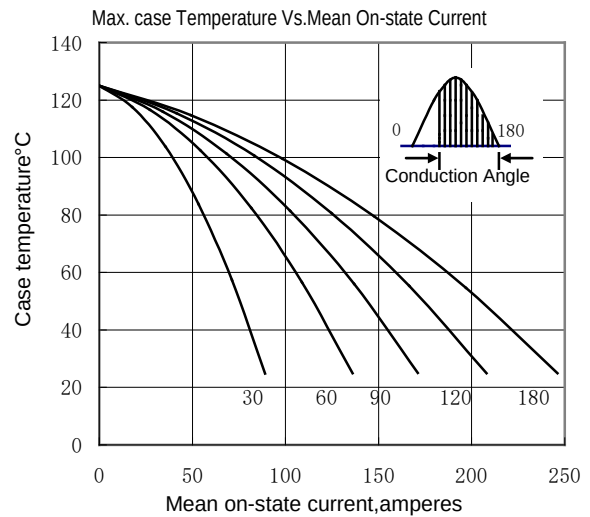


Fig.4

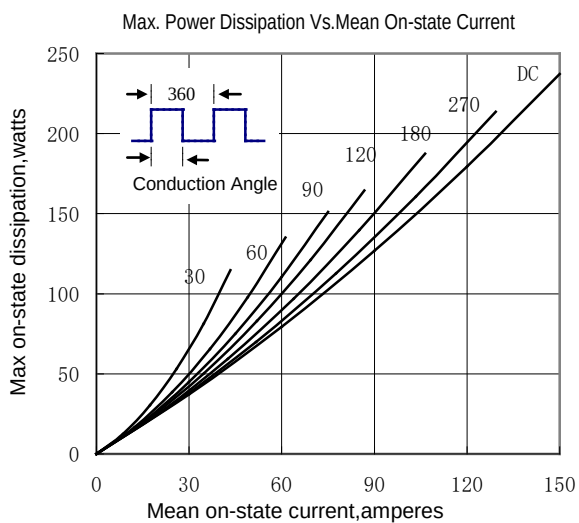


Fig.5

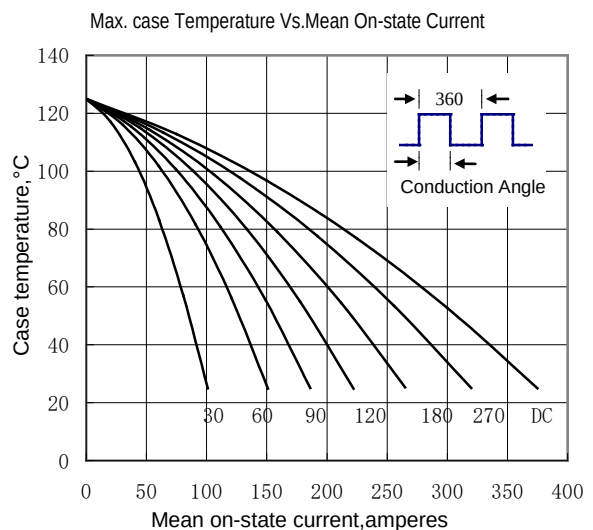


Fig.6

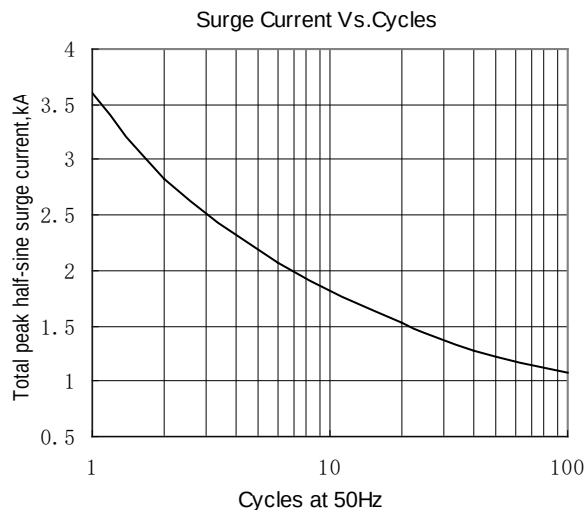


Fig.7

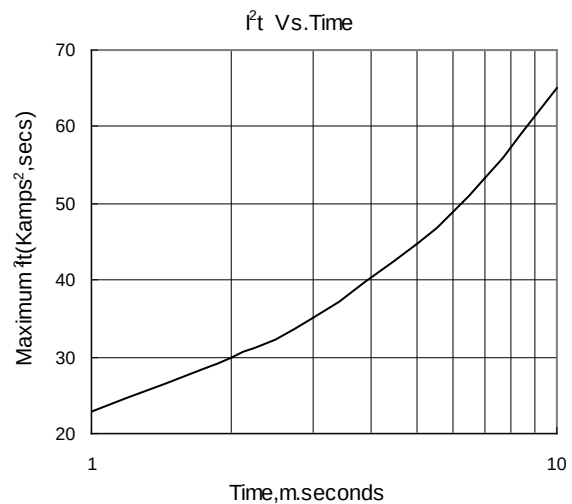


Fig.8

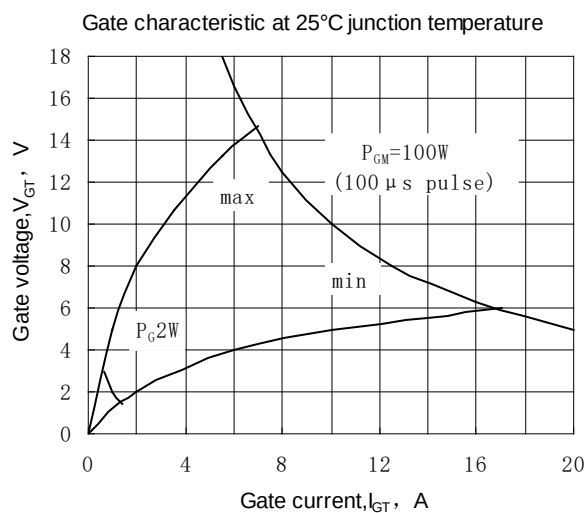


Fig.9

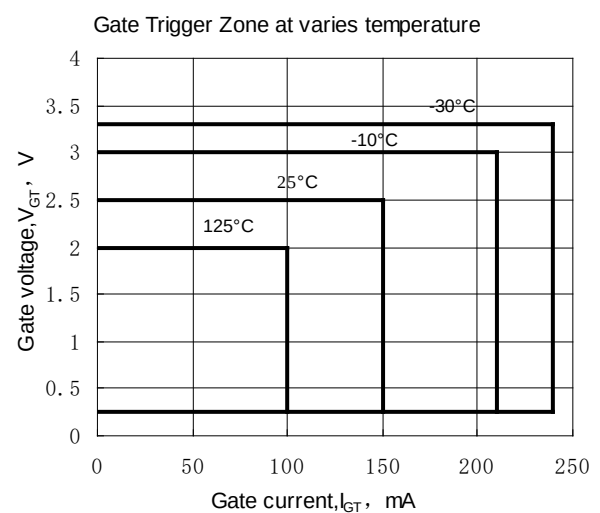


Fig.10

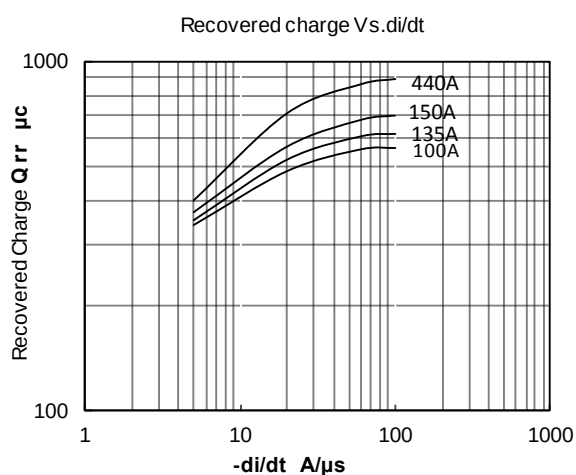


Fig.11

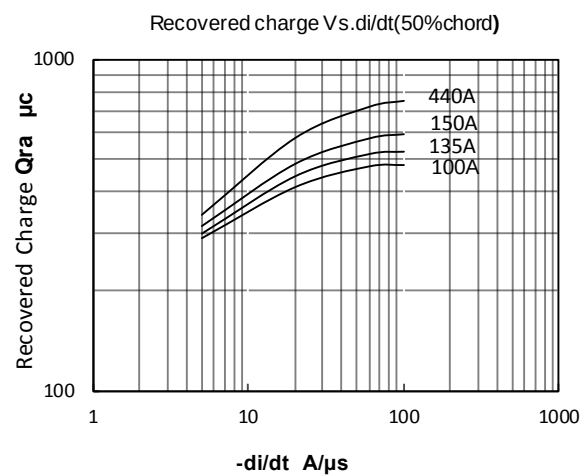


Fig.12

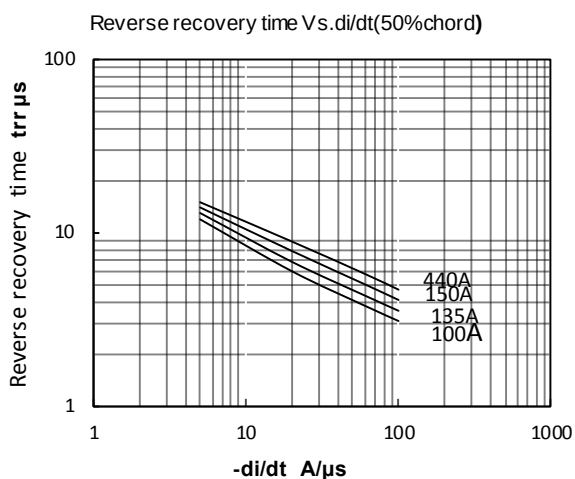


Fig.13

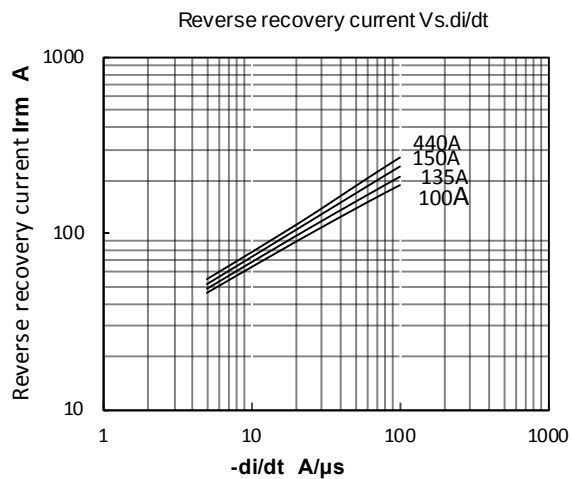
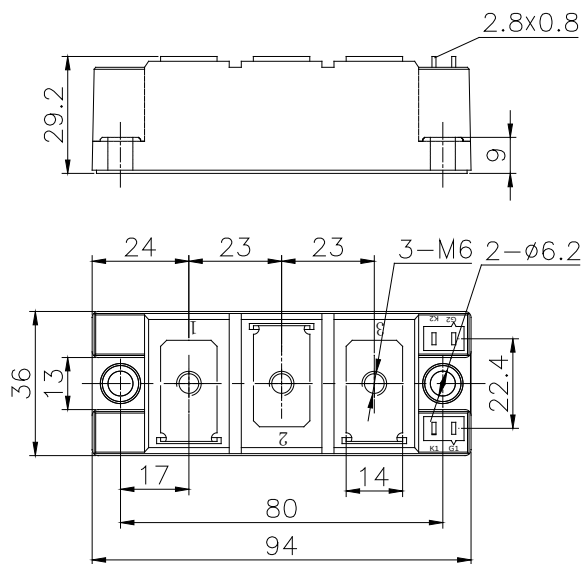
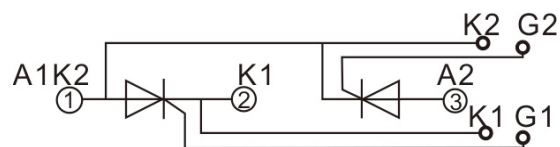


Fig.14

Outline:



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