DSKH1200

DYNSEM

Thyristor/Diode modules

Features：

- Isolated mounting base 2500V~
- Pressure contact technology with Increased power cycling capability
- Space and weight saving

Typical Applications

- AC/DC Motor drives
- Various rectifiers
- DC supply for PWM inverter

V_{DSM},V_{RSM}	V_{DRM},V_{RRM}	Type
900V	800V	DSKH 1200/08
1100V	1000V	DSKH 1200/10
1300V	1200V	DSKH 1200/12
1500V	1400V	DSKH 1200/14
1700V	1600V	DSKH 1200/16
1900V	1800V	DSKH 1200/18

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled,T_c=85°C	125			1200	A
$I_{T(RMS)}$	RMS on-state current					1884	A
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			55	mA
I_{TSM}	Surge on-state current	10ms half sine wave , V_R=0.6V_{RRM}	125			26	kA
I^2t	I^2t for fusing coordination					3380	A^2s*10^3
V_{TO}	Threshold voltage		125			0.80	V
r_T	On-state slope resistance					0.09	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=3000A	25			1.96	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=67%V_{DRM}	125			800	V/μs
di/dt	Critical rate of rise of on-state current	I_{TM} =2400A, Gate source 1.5A t_r≤0.5μs Repetitive	125			100	A/μs
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	30		200	mA
V_{GT}	Gate trigger voltage			0.8		3.0	V
I_H	Holding current			10		200	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}	125	0.2			V
$R_{th(j-c)}$	Thermal resistance Junction to case	Single side cooled per chip				0.031	°C /W
$R_{th(c-h)}$	Thermal resistance case to heatsink	Single side cooled per chip				0.020	°C /W
V_{iso}	Isolation voltage	50Hz,R.M.S,t=1min,I_{iso}:1mA(MAX)		2500			V
F_m	Terminal connection torque(M12)				14.0		N·m
	Mounting torque(M8)				12.0		N·m
T_{vj}	Junction temperature			-40		125	°C
T_{stg}	Stored temperature			-40		125	°C
W_t	Weight				3660		g

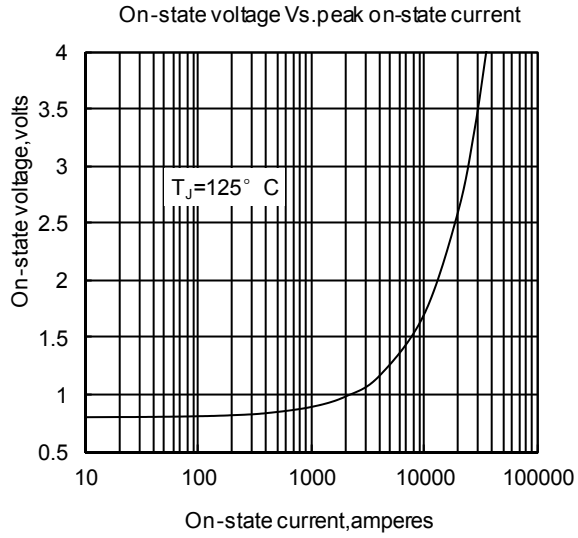


Fig1

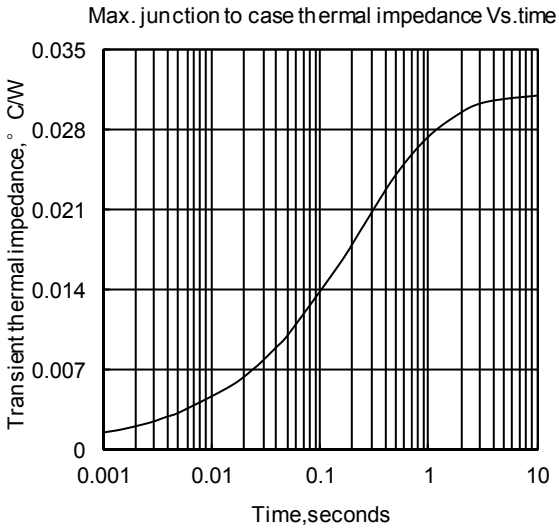


Fig2

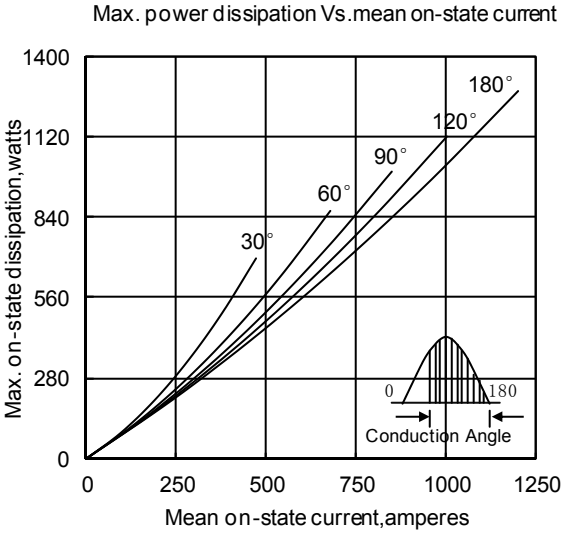


Fig3

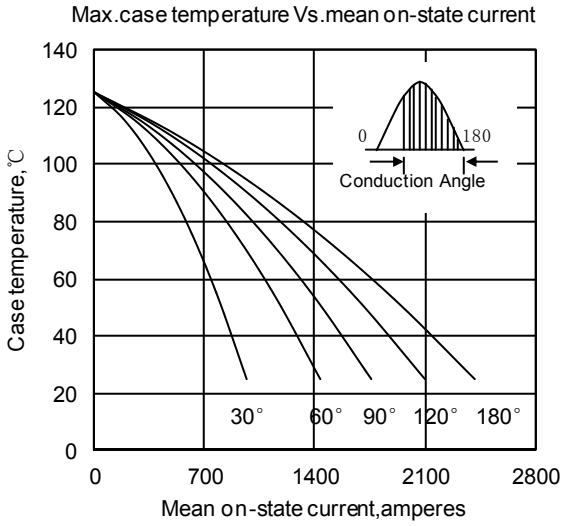


Fig4

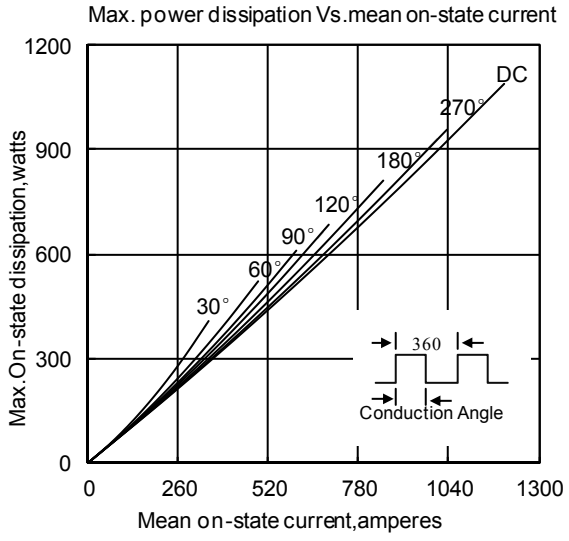


Fig5

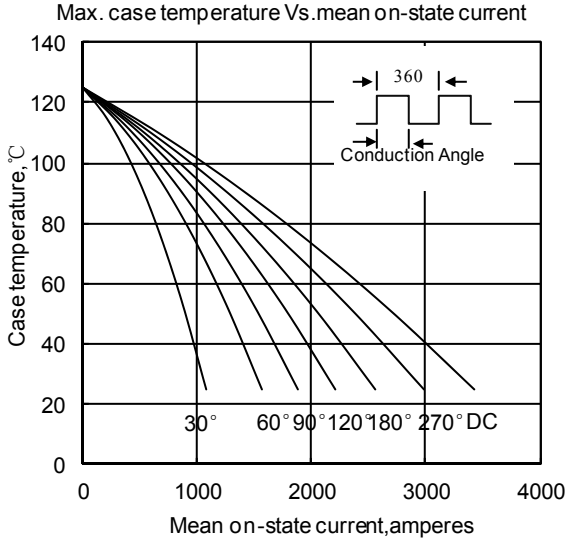


Fig6

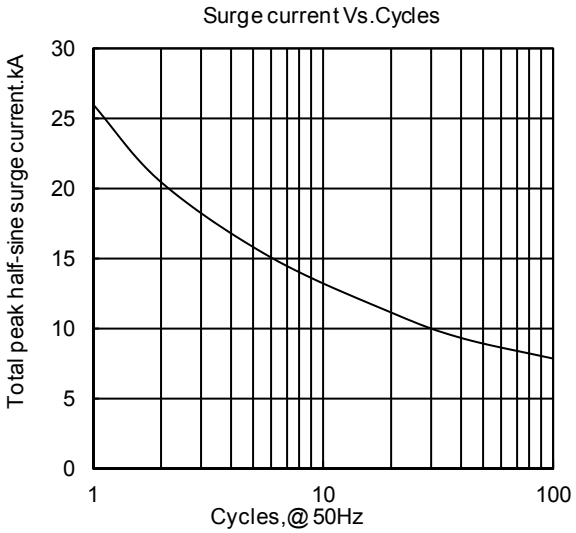


Fig7

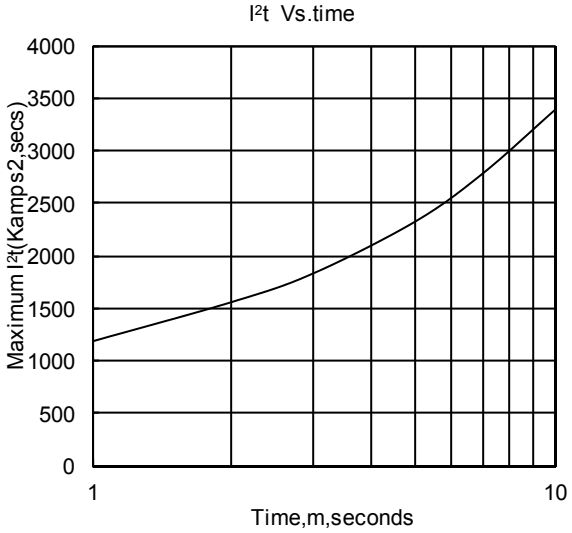


Fig8

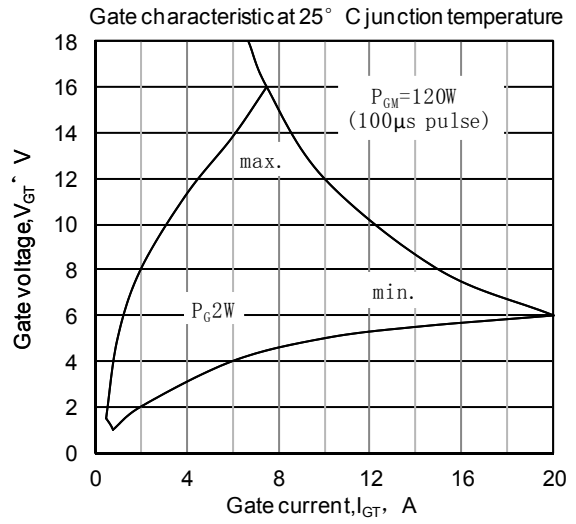


Fig9

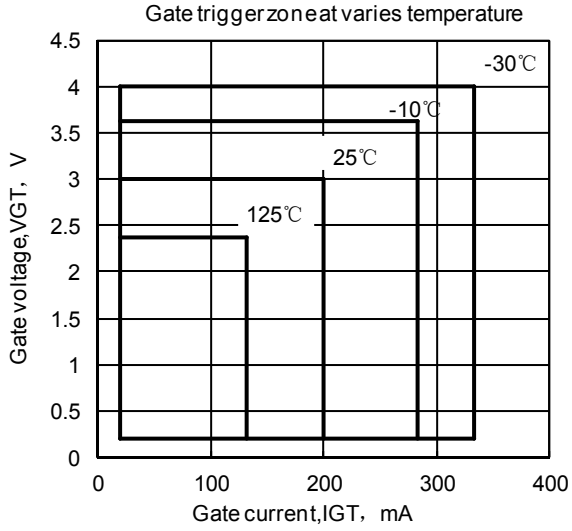
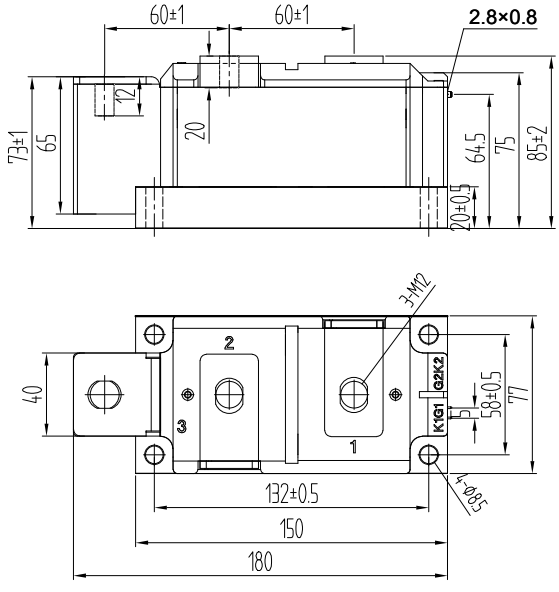


Fig10

Outline:



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